AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

Claims 1-25 (Cancelled)

26. (previously presented) A semiconductor integrated circuit formed on a single chip and comprising:

a central processing unit;

an input/output circuit; and

an internal supply voltage generating circuit,

wherein said central processing unit has a first operational mode consuming a first operational current, and a second operational mode consuming second operational current,

wherein said internal supply voltage generating circuit includes a plurality of regulators, and a control circuit controlling said regulators,

wherein said control circuit receives a first mode information signal from said central processing unit, and receives a second mode information signal from outside said

semiconductor integrated circuit via said input/output circuit, and

wherein said control circuit controls said regulators of said internal supply voltage generating circuit according to said mode information signals.

27. (previously presented) A semiconductor integrated circuit according to claim 26,

wherein said plurality of regulators include a first regulator providing said first operational current, and a second regulator providing said second operational current, said second operational current being smaller than said first operational current.

28. (previously presented) A semiconductor integrated circuit according to claim 26,

wherein said semiconductor integrated circuit receives a power supply voltage,

wherein said power supply voltage is provided to said input/output circuit and said internal supply voltage generating circuit,

wherein said internal supply voltage generating circuit is constructed to generate a plurality of internal supply voltages using said power supply voltage, and

wherein said central processing unit is selectively supplied with said plurality of internal supply voltages.

29. (previously presented) A semiconductor integrated circuit,

a central processing unit having a plurality of operation modes;

an input/output circuit constructed to receive a plurality of signals from outside;

a voltage terminal which is provided with an external supply voltage; and

a voltage generating circuit constructed to generate operation voltages according to said operation modes,

wherein said voltage terminal is coupled with said input/output circuit and said voltage generating circuit to provide said supply voltage from a first voltage line,

wherein said input/output circuit receives a mode signal from outside, and provides an operation mode control signal selectively indicating said plurality of operation modes to said voltage generating circuit,

wherein said voltage generating circuit includes a control circuit receiving said operation mode control signal, and controlling the voltage generating circuit according to the operation mode indicated by said operation mode control signal, said voltage generating circuit being coupled to said central processing unit via a second voltage line, and

wherein said plurality of operation modes include a first operation mode for which said voltage generating circuit provides a first operation voltage to said central processing unit via said second voltage line, and a second operation mode for which said voltage generating circuit provides a second operation voltage to said central processing unit via said second voltage line.

30. (previously presented) A semiconductor integrated circuit according to claim 29,

wherein said central processing unit consumes a first operation current in said first operation mode and a second operation current smaller than said first operation current in said second operation mode.

31. (previously presented) A semiconductor integrated circuit according to claim 30,

wherein said voltage supply circuit includes a first generating circuit providing said first operation current, and a second generating circuit providing said second operation current, and

wherein said control circuit controls operation of said first and second generating circuits.

32. (previously presented) A semiconductor integrated circuit according to claim 30, further comprising:

an internal volatile memory,

wherein said plurality of operation modes include a third operation mode,

wherein said voltage generating circuit is coupled to said internal volatile memory via a third voltage line to provide an operation voltage to said internal volatile memory said third operation mode.

33. (previously presented) A semiconductor integrated circuit according to claim 29,

wherein said voltage generating circuit includes a first regulator which generates said first operation voltage and a second regulator which generates said second operation voltage.

34. (previously presented) A semiconductor integrated circuit device, comprising:

a central processing unit having a plurality of operation modes;

an input/output circuit coupled to said central processing unit; and

a supply voltage generating circuit having a plurality of operation voltage outputs,

wherein said supply voltage generating circuit includes a control circuit which controls said supply voltage generating circuit to couple said operation voltage outputs to said central processing unit, selectively, depending upon the operating mode of the central processing unit.

35. (previously presented) A semiconductor integrated circuit according to claim 34, wherein said control circuit receives an operation mode control signal

and controls said supply voltage generating circuit according to the operation mode indicated by said operation mode control signal.

36. (previously presented) A semiconductor integrated circuit according to claim 35, wherein said control circuit receives said operation mode control signal from said input/output circuit.

37. (previously presented) A semiconductor integrated circuit according to claim 36, wherein said operation mode control signal is externally supplied to said input/output circuit.

38. (previously presented) A semiconductor integrated circuit according to claim 34, wherein said control circuit receives first and second operation mode control signals from said input/output circuit and said central processing unit, respectively, and controls said voltage generating circuit according to respective operation modes indicated by said first and second operation mode control signals.

39. (currently amended) A semiconductor integrated circuit according to claim 34, wherein ~~Wherein said~~ plurality of operation modes include a first operation mode in which a first of said operation voltage outputs is coupled to said central processing unit to provide a first operating current, and a second operation mode in which a second of said operation voltage outputs is coupled to said central processing unit to provide a second operating current smaller than said first operating current.

40. (previously presented) A semiconductor integrated circuit according to claim 39, wherein said first and second operation voltage outputs are outputs of first and second regulators, respectively.

41. (previously presented) A semiconductor integrated circuit according to claim 39, further comprising:

an internal volatile memory, and

wherein said first and second operation voltage output terminals are coupled to said internal volatile memory via a dedicated voltage supply line for said internal volatile

memory in said first and second operation modes, respectively.

42. (previously presented) A semiconductor integrated circuit according to claim 41, wherein said plurality of operation modes include a third operation mode, and wherein said supply voltage generating circuit has an additional operation voltage output which is coupled to said internal volatile memory via said additional voltage line in said third operating mode.

43. (previously presented) A semiconductor integrated circuit according to claim 42, wherein said additional operation voltage output is an output of a third regulator.